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Question Paper Code : 20447

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2018.

Third Semester

Electrical and Electronics Engineering

EE 6301 — DIGITAL LOGIC CIRCUITS

(Common to: Electronics and Instrumentation Engineering/
Instrumentation and Control Engineering)

(Regulations 2013)

(Also Common to: PTEE 6301 — Digital Logic Circuits for B.E. (Part-Time) – Third Semester – Electrical and Electronics Engineering – Regulations 2014)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert $(115)_{10}$ and $(235)_{10}$ to hexadecimal numbers.

2. Write about a gray code and mention it's advantages.

3. Define K-map.

4. Compare decoder and Demultiplexer.

5. Mention about race around condition in a flip-flop.

6. What is a presettable counter and ripple counter?

7. What happens to the information stored in a memory location after it has been read and write operation?

8. What is Programmable Logic Array?

9. Define modularity.

10. List the languages that are combined together to get VHDL language.

PART B — (5 × 13 = 65 marks)

11. (a) Explain in detail about error detecting and error correcting code. (13)

Or

(b) Write short notes on following :

(i) RTL,

(ii) DTL,

(iii) TTL and

(iv) ECL. (13)

12. (a) (i) Plot the logical expression $ABCD + A\overline{B}\,\overline{C}\,\overline{D} + A\overline{B}C + AB$ on a 4-variable K-map; obtain the simplified expression from the map. (7)

(ii) Express the function $Y = A + \overline{B}C$ in canonical SOP and canonical POS form. (6)

Or

(b) Design a 4-bit gray code to binary converter and express using logic gates. (13)

13. (a) Explain the operation, state diagram and characteristics of T flip-flop and master-slave JK flip-flop. (13)

Or

(b) Explain in detail about different shift registers. (13)

14. (a) Discuss about the hazards in asynchronous sequential circuit and the ways to eliminate them. (13)

Or

(b) Design an asynchronous circuit that will operate only for the first pulse received whenever a control input is asserted from LOW to HIGH state. Further pulses will be ignored. (13)

15. (a) Implement a full adder circuit using PLA having three inputs, eight product terms, and two outputs. (13)

Or

(b) Briefly explain the operations involved using RAM and compare Static RAM and Dynamic RAM. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Design a logic circuit that has three inputs, A, B, C and whose output will be HIGH only when a majority of the inputs are HIGH. (15)

Or

(b) Apply K-map and simplify the following.

$y = \overline{C}\left(\overline{ABD} + D\right) + A\overline{B}C + \overline{D}$ (15)

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